REMARKS

This application has been reviewed in light of the Office Action dated March 24, 2004. Claims 1, 2, 4-6 and 10-18 are presented for examination. Claims 3, 7-9, and 19-22 have been canceled, without prejudice or disclaimer of subject matter. Claims 1, 2, 4-6 and 10-18 have been amended to define more clearly what Applicants regard as their invention. Claims 1 and 11 are in independent form. Favorable reconsideration is requested.

The title has been amended to make it more descriptive, as required in the Office Action.

Claims 1 and 11 have been amended as suggested by the Examiner in response to the objection thereto.

Applicants note with appreciation the indication that Claims 13 and 15-17 would be allowable if rewritten so as not to depend from a rejected claim, and with no change in scope. The latter claims have not been so rewritten because, for the reasons given below, their base claim is believed to be allowable.

Claims 5, 6, 8 and 9 were rejected under 35 U.S.C. § 112, second paragraph, as indefinite.

First, cancellation of Claims 8 and 9 renders the rejections of those claims moot.

The claims have been carefully reviewed and amended as deemed necessary to ensure that they conform fully to the requirements of Section 112, second paragraph, with special attention to the points raised in paragraph 10 of the Office Action. Specifically, Claim 5 and 6 have been amended to depend from Claim 4, which recites a

plurality of wirings for supplying the reference voltage and provides antecedent basis for the wirings recited in Claim 5 and 6. It is believed that the rejection under Section 112, second paragraph, has been obviated, and its withdrawal is therefore respectfully requested.

Claims 1-6, 10, 11 and 18 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,051,857 ("Miida"). Claim 7 was rejected under 35 U.S.C. § 103(a) as being obvious from Miida in view of U.S. Patent 4,149,192 ("Takenuchi"). Claims 12 and 14 were rejected as obvious over Miida in view of JP 58-137243 ("Kunihiro"), and Claims 19-22 were rejected as obvious over Miida in view of U.S. Patent No. 5,734,457 ("Mitsui").

Claim 1 is directed to a solid-state imaging device of an amplification type that includes a plurality of picture elements arranged two-dimensionally. Each picture element includes a semiconductor light-receiving region of a first conductivity type serving as a photoelectric conversion element. The light-receiving region is disposed in a common well comprising a semiconductor of a second conductivity type. A semiconductor region of the first conductivity type serves as a source and drain of a transistor for amplification, the semiconductor region being disposed in the common well. A plurality of contacts are provided for supplying a reference voltage to the common well, and the plurality of contacts are disposed between the picture elements or within the picture elements. Among other advantages provided by this combination of features is that shading can be reduced by controlling the distribution of potential in the common well, which becomes a back gate potential for the amplification transistor.

Miida relates to an imaging device in which holes are photogenerated in a well region 15 of a photodiode, and these holes are transferred through the well region 15

to a heavily doped layer 25, which is formed in the well region 15 near the gate region of the amplification transistor, thereby changing the potential of the gate and providing an output signal from the source 16. Thus, the common well 15 of Miida operates in a floating state. The well 15 is formed of a p-type semiconductor region, and an n+ type semiconductor light-receiving region 17 serves as a photoelectric conversion element formed in the well. A semiconductor region n+ region 17a serves as drain of the transistor for amplification. Contacts are provided for supplying a reference voltage to the common well are provided inside the picture element array area in the common well.

The Examiner is understood to cite the drain (17a) of the amplification transistor as corresponding to the claimed contact. However, because the drain (17a) is an impurity region of n+ type, this region supplies a reference voltage into the n-type layer 12 (which corresponds, in a sense, to the substrate of the present invention) formed under the common well, rather than into the p-type common well. Thus, Miida is not seen as teaching or suggesting contacts that supply a reference voltage to a common well in which the source and drain of a transistor for amplification are formed, the contacts being disposed between the picture elements or within the picture elements, as recited in Claim 1.

Accordingly, Claim is believed to be patentable over Miida.

Independent Claim 11 recites features similar to those discussed above with respect to Claim 1 and therefore is also believed to be patentable over Miida for the reasons discussed above.

A review of the other art of record has failed to reveal anything which, in Applicants' opinion, would remedy the deficiencies of the art discussed above, as

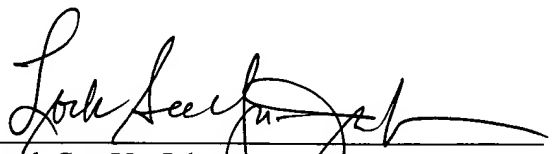
references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration or reconsideration, as the case may be, of the patentability of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration and early passage to issue of the present application.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,



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